I have amended claims 28 & 37 by changing some words, phrases and rearrangement of them, which is simply English language modification in the latest copy of record. This amendment does not add any new material claimed other the prior art and some English words, phrases and rearrangement of them. Particularly in currently amended claim-37, I have added underlined words, only to increase clarity without adding any new material claimed, as in the following:

"Wherein I/O adapter/control units in plurality and different one of which is coupled directly to each .."

The above added underlined words in currently amended claim-37 do not add any new material claimed, it was described in as field application wherein the description paragraph with the heading **"Distributed Computing Architecture"** is provided in the following for the consideration of the examiner. The same paragraph is on page-18 in the International Publication Number **WO 2006/037231 A1**, and it is the paragraph # [068] in the latest copy of record with USPTO communicated in January 2010. Please note highlighted (bold) words in the above stated paragraph placed in double square brackets in the following.

[[Distributed Computing Architecture

The parallel computer architecture depicted in Fig. 4 land itself into distributed computing architecture. This is achieved when each processor and associated memory forming a self-contained computer in itself is physically located at each network node or a substation, and communicate over communication lines with commonly shared memory and server processor both located at central station or load dispatch center in a power network. **It is possible to have an input/output unit with a computer at each network node or substation, which can be used to read local sub-network data in parallel** and communicate over communication line to commonly shared memory for the formation and storage of network wide global data at the central load dispatch center in the power network.]]

Equations (35) to (39) in claim-28 that follows requires square root sign. Please note correctly highlighted (bold) complex variables in eq. (30) and (35). The highlighting (bold) of complex variables could be wrong in Examiner's amendment and any of my prior correspondences.

Drawings:

Examiner's amendments are incorporated in all drawings. In PCT application I had indicated Fig.2, Fig. 3a, Fig. 3b, and Fig. 4 for publication along with abstract on first page. However, **based on new title of the allowed application, I would like that Fig. 3b and Fig. 4 should be published in granted patent because they involve contents of allowed claims 28, 30, and 37.**

Comments on statement of reasons for allowance:

Statement of reasons, it is strongly believed, should also state invented broadly claimed multiprocessor computing apparatus for performing parallel loadflow computation (or any other parallel computation or processing) using the method of Suresh's diakoptics for tearing

big network (big computation problem) into small sub-networks (small sub-problems). The broadly claimed multiprocessor computing apparatus is a breakthrough parallel computer architecture, and marks the beginning of the new era of universal multiprocessing computation as is evident from as filed application. The claimed invented multiprocessor computing apparatus can be used for many other applications, and many more others can be formulated for better performance on the invented broadly claimed multiprocessor computing apparatus. I think **an inventor is entitled to claim his invention as broadly as possible.** As was originally stated by this inventor that the broadly claimed multiprocessor computing apparatus is the best possible parallel computer architecture though there could be variations in micro architecture details.

Cited References

I believe that all the references cited in the examination process in different Office Actions will be included in publication of the granted patent. **At least two more reference listed in the following needs to be cited to further show the state of the art with respect to the Parallel Loadflow Computation and Multiprocessor Computing Apparatus:**

1. Shin-Der Chen, Jiann-Fuh Chen, "Fast loadflow using multiprocessors", Electrical Power & Energy Systems, 22 (2000) 231-236. **(Originally cited by me in as filed application)**
2. DeRoo, "Method and Apparatus for Arbitrating Access Requests to a Memory", US Patent No.: 6182196B1, dated January 30, 2001. **(Cited by the Examiner in his Notice of Office Action dated February 25, 2009)**

This response is respectfully prepared to further refine the allowed application. Hope, the final refinements described in the above will be positively considered by the examiner and included in the publication of the allowed application.

Sincerely,

Suresh Patel

Enclosures: Amended Drawings (14-Pages) + this cover letter & Amended Claims 1-37 listed in ascending order (8-pages) + PART B – Fees Transmittal & Credit Card Payment forms (2-pages) = total 24-pages

Note: I love America, its founding fathers, leaders, and people. In allowance of my patent applications, now I have first hand experience as to why America is the world leader. Long Live America! This sick world is badly in need of your leadership. Moreover, I encourage businesses to use technologies of any of my patent applications and decide what I deserved to be paid.

Note: All examiner's Amendments are accepted.